4.22. Port Controller(CPU-PORT)

The chip has 7 ports for multi-functional input/out pins. They are shown below:

- Port A(PA): 22 input/output port
- Port C(PC): 19 input/output port
- Port D(PD): 18 input/output port
- Port E(PE) : 16 input/output port
- Port F(PF) : 7 input/output port
- Port G(PG) : 14 input/output port
- Port L(PL) : 12 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions are not used. The total 2 group external PIO interrupt sources are supported and interrupt mode can be configured by software.

4.22.1. Port Controller Register List

Module Name	Base Address
PIO	0x01C20800

Register Name	Offset	Description
Pn_CFG0	n*0x24+0x00	Port n Configure Register 0 (n from 0 to 6)
Pn_CFG1	n*0x24+0x04	Port n Configure Register 1 (n from 0 to 6)
Pn_CFG2	n*0x24+0x08	Port n Configure Register 2 (n from 0 to 6)
Pn_CFG3	n*0x24+0x0C	Port n Configure Register 3 (n from 0 to 6)
Pn_DAT	n*0x24+0x10	Port n Data Register (n from 0 to 6)
Pn_DRV0	n*0x24+0x14	Port n Multi-Driving Register 0 (n from 0 to 6)
Pn_DRV1	n*0x24+0x18	Port n Multi-Driving Register 1 (n from 0 to 6)
Pn_PUL0	n*0x24+0x1C	Port n Pull Register 0 (n from 0 to 6)
Pn_PUL1	n*0x24+0x20	Port n Pull Register 1 (n from 0 to 6)
PA_INT_CFG0	0x200+0*0x20+0x00	PIO Interrrupt Configure Register 0
PA _INT_CFG1	0x200+0*0x20+0x04	PIO Interrrupt Configure Register 1
PA _INT_CFG2	0x200+0*0x20+0x08	PIO Interrrupt Configure Register 2
PA _INT_CFG3	0x200+0*0x20+0x0C	PIO Interrrupt Configure Register 3
PA _INT_CTL	0x200+0*0x20+0x10	PIO Interrupt Control Register
PA _INT_STA	0x200+0*0x20+0x14	PIO Interrupt Status Register
PA_INT_DEB	0x200+0*0x20+0x18	PIO Interrupt Debounce Register
PG_INT_CFG0	0x200+1*0x20+0x00	PIO Interrrupt Configure Register 0
PG _INT_CFG1	0x200+1*0x20+0x04	PIO Interrrupt Configure Register 1
PG _INT_CFG2	0x200+1*0x20+0x08	PIO Interrrupt Configure Register 2
PG _INT_CFG3	0x200+1*0x20+0x0C	PIO Interrrupt Configure Register 3

PG _INT_CTL	0x200+1*0x20+0x10	PIO Interrupt Control Register
PG _INT_STA	0x200+1*0x20+0x14	PIO Interrupt Status Register
PG _INT_DEB	0x200+1*0x20+0x18	PIO Interrupt Debounce Register

4.22.2. Port Controller Register Description

4.22.2.1. PA Configure Register 0 (Default Value: 0x77777777)

Offset: 0x00			Register Name: **PA_CFG0_REG**
Bit	R/W	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PA7_SELECT 000:Input 001:Output 010:SIM_CLK 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PA6_SELECT 000:Input 001:Output 010:SIM_PWREN 011: Reserved 100:Reserved 101:Reserved 110:PA_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PA5_SELECT 000:Input 001:Output 010:UART0_RX 011:PWM0 100:Reserved 101:Reserved 110:PA_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PA4_SELECT 000:Input 001:Output 010:UART0_TX 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PA3_SELECT 000:Input 001:Output 010:UART2_CTS 011:JTAG_DI 100:Reserved 101:Reserved 110:PA_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PA2_SELECT 000:Input 001:Output

			010:UART2_RTS 011:JTAG_DO 100:Reserved 101:Reserved 110:PA_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PA1_SELECT 000:Input 001:Output 010:UART2_RX 011:JTAG_CK 100:Reserved 101:Reserved 110:PA_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PA0_SELECT 000:Input 001:Output 010:UART2_TX 011:JTAG_MS 100:Reserved 101:Reserved 110:PA_EINT0 111:IO Disable

4.22.2.2. PA Configure Register 1 (Default Value: 0x77777777)

Offset: 0x04			Register Name: **PA_CFG1_REG**
Bit	R/W	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PA15_SELECT 000:Input 001:Output 010:SPI1_MOSI 011:UART3_RTS 100:Reserved 101:Reserved 110:PA_EINT15 111:IO Disable
27	/	/	
26:24	R/W	0x7	PA14_SELECT 000:Input 001:Output 010:SPI1_CLK 011:UART3_RX 100:Reserved 101:Reserved 110:PA_EINT14 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PA13_SELECT 000:Input 001:Output 010:SPI1_CS 011:UART3_TX 100:Reserved 101:Reserved 110:PA_EINT13 111:IO Disable
19	/	/	
18:16	R/W	0x7	PA12_SELECT 000:Input 001:Output 010:TWI0_SDA 011:DI_RX 100:Reserved 101:Reserved 110:PA_EINT12 111:IO Disable

15	/	/	
14:12	R/W	0x7	PA11_SELECT 000:Input 001:Output 010:TWI0_SCK 011:DI_TX 100:Reserved 101:Reserved 110:PA_EINT11 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PA10_SELECT 000:Input 001:Output 010:SIM_DET 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT10 111:IO Disable
7	/	/	
6:4	R/W	0x7	PA9_SELECT 000:Input 001:Output 010:SIM_RST 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT9 111:IO Disable
3	/	/	
2:0	R/W	0x7	PA8_SELECT 000:Input 001:Output 010:SIM_DATA 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT8 111:IO Disable

4.22.2.3. PA Configure Register 2 (Default Value: 0x00777777)

Offset: 0x08			Register Name: **PA_CFG2_REG**
Bit	R/W	Default/Hex	Description
31:23	/	/	
22:20	R/W	0x7	PA21_SELECT 000:Input 001:Output 010:PCM0_DIN 011:SIM_VPPPP 100:Reserved 101:Reserved 110:PA_EINT21 111:IO Disable
19	/	/	
18:16	R/W	0x7	PA20_SELECT 000:Input 001:Output 010:PCM0_DOUT 011:SIM_VPPEN 100:Reserved 101:Reserved 110:PA_EINT20 111:IO Disable
15	/	/	
14:12	R/W	0x7	PA19_SELECT 000:Input 001:Output

			010:PCM0_CLK 011:TWI1_SDA 100:Reserved 101:Reserved 110:PA_EINT19 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PA18_SELECT 000:Input 001:Output 010:PCM0_SYNC 011:TWI1_SCK 100:Reserved 101:Reserved 110:PA_EINT18 111:IO Disable
7	/	/	
6:4	R/W	0x7	PA17_SELECT 000:Input 001:Output 010:OWA_OUT 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT17 111:IO Disable
3	/	/	
2:0	R/W	0x7	PA16_SELECT 000:Input 001:Output 010:SPI1_MISO 011:UART3_CTS 100:Reserved 101:Reserved 110:PA_EINT16 111:IO Disable

4.22.2.4. PA Configure Register 3 (Default Value: 0x00000000)

Offset: 0x0C			Register Name: **PA_CFG3_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.5. PA Data Register (Default Value: 0x00000000)

Offset: 0x10			Register Name: **PA_DATA_REG**
Bit	R/W	Default/Hex	Description
31:22	/	/	/
21:0	R/W	0x0	PA_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.22.2.6. PA Multi-Driving Register 0 (Default Value: 0x55555555)

Offset: 0x14			Register Name: **PA_DRV0_REG**
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.2.7. PA Multi-Driving Register 1 (Default Value: 0x00000555)

Offset: 0x18			Register Name: **PA_DRV1 _REG**
Bit	R/W	Default/Hex	Description
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 16~21) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.2.8. PA PULL Register 0 (Default Value: 0x00000000)

Offset: 0x1C			Register Name: **PA_PULL0_REG**
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.2.9. PA PULL Register 1 (Default Value: 0x00000000)

Offset: 0x20			Register Name: **PA_PULL1_REG**
Bit	R/W	Default/Hex	Description
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 16~21) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.2.10. PC Configure Register 0 (Default Value: 0x77777777)

Offset: 0x48			Register Name: **PC_CFG0_REG**
Bit	R/W	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PC7_SELECT 000:Input 001:Output 010:NAND_RB1 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PC6_SELECT 000:Input 001:Output 010:NAND_RB0 011:SDC2_CMD 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PC5_SELECT 000:Input 001:Output 010:NAND_RE 011:SDC2_CLK 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PC4_SELECT 000:Input 001:Output 010:NAND_CE0 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PC3_SELECT 000:Input 001:Output 010:NAND_CE1 011:SPI0_CS 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PC2_SELECT 000:Input 001:Output 010:NAND_CLE 011:SPI0_CLK 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PC1_SELECT 000:Input 001:Output 010:NAND_ALE 011:SPI0_MISO

			100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PC0_SELECT 000:Input 001:Output 010:NAND_WE 011:SPI0_MOSI 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.22.2.11. PC Configure Register 1 (Default Value: 0x77777777)

Offset: 0x4C			Register Name: **PC_CFG1_REG**
Bit	R/W	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PC15_SELECT 000:Input 001:Output 010:NAND_DQ7 011:SDC2_D7 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PC14_SELECT 000:Input 001:Output 010:NAND_DQ6 011:SDC2_D6 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PC13_SELECT 000:Input 001:Output 010:NAND_DQ5 011:SDC2_D5 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PC12_SELECT 000:Input 001:Output 010:NAND_DQ4 011:SDC2_D4 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PC11_SELECT 000:Input 001:Output 010:NAND_DQ3 011:SDC2_D3 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/

10:8	R/W	0x7	PC10_SELECT 000:Input 001:Output 010:NAND_DQ2 011:SDC2_D2 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PC9_SELECT 000:Input 001:Output 010:NAND_DQ1 011:SDC2_D1 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PC8_SELECT 000:Input 001:Output 010:NAND_DQ0 011:SDC2_D0 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.22.2.12. PC Configure Register 2 (Default Value: 0x00000777)

Offset: 0x50			Register Name: **PC_CFG2_REG**
Bit	R/W	Default/Hex	Description
31:11	/	/	/
10:8	R/W	0x7	/
7	/	/	/
6:4	R/W	0x7	/
3	/	/	/
2:0	R/W	0x7	PC16_SELECT 000:Input 001:Output 010:NAND_DQS 011:SDC2_RST 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.22.2.13. PC Configure Register 3 (Default Value: 0x00000000)

Offset: 0x54			Register Name: **PC_CFG3_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.14. PC Data Register (Default Value: 0x00000000)

Offset: 0x58			Register Name: **PC_DATA_REG**
Bit	R/W	Default/Hex	Description
31:19	/	/	/
18:0	R/W	0x0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.22.2.15. PC Multi-Driving Register 0 (Default Value: 0x55555555)

Offset: 0x5C			Register Name: **PC_DRV0_REG**
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PC_DRV PC[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.2.16. PC Multi-Driving Register 1 (Default Value: 0x00000015)

Offset: 0x60			Register Name: **PC_DRV1_REG**
Bit	R/W	Default/Hex	Description
31:6	/	/	/
[2i+1:2i] (i=0~2)	R/W	0x1	PC_DRV PC[n] Multi-Driving Select (n = 16~18) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.2.17. PC PULL Register 0 (Default Value: 0x00005140)

Offset: 0x64			Register Name: **PC_PULL0_REG**
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x5140	PC_PULL PC[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.2.18. PC PULL Register 1 (Default Value: 0x00000014)

Offset: 0x68			Register Name: **PC_PULL1_REG**
Bit	R/W	Default/Hex	Description
31:6	/	/	Reserved
[2i+1:2i] (i=0~2)	R/W	0x14	PC_PULL PC[n] Pull-up/down Select (n = 16~18) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.2.19. PD Configure Register 0 (Default Value: 0x77777777)

Offset: 0x6C			Register Name: **PD_CFG0_REG**
Bit	R/W	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PD7_SELECT 000:Input 001:Output 010:RGMII_TXD3/MII_TXD3/RMII_NULL 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	Reserved
26:24	R/W	0x7	PD6_SELECT 000:Input 001:Output 010:RGMII_NULL/MII_RXERR/RMII_RXER 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PD5_SELECT 000:Input 001:Output 010:RGMII_RXCTL/MII_RXDV/RMII_NULL 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PD4_SELECT 000:Input 001:Output 010:RGMII_RXCK/MII_RXCK/RMII_NULL 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PD3_SELECT 000:Input 001:Output 010:RGMII_RXD0/MII_RXD0/RMII_RXD0 011:Reserved 100:Reserved 101:Reserved

			110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PD2_SELECT 000:Input 001:Output 010:RGMII_RXD1/MII_RXD1/RMII_RXD1 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PD1_SELECT 000:Input 001:Output 010:RGMII_RXD2/MII_RXD2/RMII_NULL 011:DI_RX 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD0_SELECT 000:Input 001:Output 010:RGMII_RXD3/ MII_RXD3/ RMII_NULL 011:DI_TX 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.22.2.20. PD Configure Register 1 (Default Value: 0x77777777)

Offset: 0x70			Register Name: **PD_CFG1_REG**
Bit	R/W	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PD15_SELECT 000:Input 001:Output 010:RGMII_CLKIN/MII_COL/RMII_NULL 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PD14_SELECT 000:Input 001:Output 010:RGMII_NULL/MII_TXERR/RMII_NULL 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PD13_SELECT 000:Input 001:Output 010:RGMII_TXCTL/MII_TXEN/RMII_TXEN 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PD12_SELECT

			000:Input 001:Output 010:RGMII_TXCK/MII_TXCK/RMII_TXCK 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PD11_SELECT 000:Input 001:Output 010:RGMII_NULL/MII_CRS/RMII_NULL 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PD10_SELECT 000:Input 001:Output 010:RGMII_TXD0/MII_TXD0/RMII_TXD0 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PD9_SELECT 000:Input 001:Output 010:RGMII_TXD1/MII_TXD1/RMII_TXD1 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD8_SELECT 000:Input 001:Output 010:RGMII_TXD2/MII_TXD2/RMII_NULL 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.22.2.21. PD Configure Register 2 (Default Value: 0x00000077)

Offset: 0x74			Register Name: **PD_CFG2_REG**
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x7	PD17_SELECT 000:Input 001:Output 010:MDIO 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD16_SELECT 000:Input 001:Output 010:MDC 011:Reserved 100:Reserved 101:Reserved

			110:Reserved 111:IO Disable

4.22.2.22. PD Configure Register 3 (Default Value: 0x00000000)

Offset: 0x78			Register Name: **PD_CFG3_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.23. PD Data Register (Default Value: 0x00000000)

Offset: 0x7C			Register Name: **PD_DATA _REG**
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:0	R/W	0x0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.22.2.24. PD Multi-Driving Register 0 (Default Value: 0x55555555)

Offset: 0x80			Register Name: **PD_DRV0_REG**
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PD_DRV PD[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.2.25. PD Multi-Driving Register 1 (Default Value: 0x00000005)

Offset: 0x84			Register Name: **PD_DRV1_REG**
Bit	R/W	Default/Hex	Description
31:4	/	/	/
[2i+1:2i] (i=0~1)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 16~17) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.2.26. PD PULL Register 0 (Default Value: 0x00000000)

Offset: 0x88			Register Name: **PD_PULL0_REG**
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.2.27. PD PULL Register 1 (Default Value: 0x00000000)

Offset: 0x8C			Register Name: **PD_PULL1_REG**
Bit	R/W	Default/Hex	Description
31:4	/	/	Reserved
[2i+1:2i] (i=0~1)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 16~17) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.2.28. PE Configure Register 0 (Default Value: 0x77777777)

Offset: 0x90			Register Name: **PE_CFG0_REG**
Bit	R/W	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PE7_SELECT 000:Input 001:Output 010:CSI_D3 011:TS_D3 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PE6_SELECT 000:Input 001:Output 010:CSI_D2 011:TS_D2 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PE5_SELECT 000:Input 001:Output 010: CSI_D1 011:TS_D1 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/

18:16	R/W	0x7	PE4_SELECT 000:Input 001:Output 010: CSI_D0 011:TS_D0 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PE3_SELECT 000:Input 001:Output 010:CSI_VSYNC 011:TS_DVLD 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PE2_SELECT 000:Input 001:Output 010:CSI_HSYNC 011:TS_SYNC 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PE1_SELECT 000:Input 001:Output 010:CSI_MCLK 011:TS_ERR 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PE0_SELECT 000:Input 001:Output 010:CSI_PCLK 011:TS_CLK 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.22.2.29. PE Configure Register 1 (Default Value: 0x77777777)

Offset: 0x94			Register Name: **PE_CFG1_REG**
Bit	R/W	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PE15_SELECT 000:Input 001:Output 010: Reserved 011: Reserved 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PE14_SELECT 000:Input 001:Output 010: Reserved 011: Reserved

			100: Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PE13_SELECT 000:Input 001:Output 010: CSI_SDA 011: TWI2_SDA 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PE12_SELECT 000:Input 001:Output 010: CSI_SCK 011: TWI2_SCK 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PE11_SELECT 000:Input 001:Output 010:CSI_D7 011: TS_D7 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PE10_SELECT 000:Input 001:Output 010:CSI_D6 011: TS_D6 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PE9_SELECT 000:Input 001:Output 010:CSI_D5 011: TS_D5 100: Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PE8_SELECT 000:Input 001:Output 010:CSI_D4 011: TS_D4 100: Reserved 101:Reserved 110:Reserved 111:IO Disable

4.22.2.30. PE Configure Register 2 (Default Value: 0x00000000)

Offset: 0x98			Register Name: **PE_CFG2_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.31. PE Configure Register 3 (Default Value: 0x00000000)

Offset: 0x9C			Register Name: **PE_CFG3_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.32. PE Data Register (Default Value: 0x00000000)

Offset: 0xA0			Register Name: **PE_DATA _REG**
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.22.2.33. PE Multi-Driving Register 0 (Default Value: 0x55555555)

Offset: 0xA4			Register Name: **PE_DRV0_REG**
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PE_DRV PE[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.2.34. PE Multi-Driving Register 1 (Default Value: 0x00000000)

Offset: 0xA8			Register Name: **PE_DRV1_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.35. PE PULL Register 0 (Default Value: 0x00000000)

Offset: 0xAC			Register Name: **PE_PULL0_REG**
Bit	R/W	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x0	PE_PULL PE[n] Pull-up/down Select (n = 0~15)

			00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.2.36. PE PULL Register 1 (Default Value: 0x00000000)

Offset: 0xB0			Register Name: **PE_PULL1_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.37. PF Configure Register 0 (Default Value: 0x07373733)

Offset: 0xB4			Register Name: **PF_CFG0_REG**
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x7	PF6_SELECT 000:Input 001:Output 010: Reserved 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23			
22:20	R/W	0x3	PF5_SELECT 000:Input 001:Output 010:SDC0_D2 011:JTAG_CK 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PF4_SELECT 000:Input 001:Output 010:SDC0_D3 011:UART0_RX 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x3	PF3_SELECT 000:Input 001:Output 010:SDC0_CMD 011:JTAG_DO 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PF2_SELECT 000:Input 001:Output 010:SDC0_CLK 011:UART0_TX 100:Reserved 101:Reserved

			110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x3	PF1_SELECT 000:Input 001:Output 010:SDC0_D0 011:JTAG_DI 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x3	PF0_SELECT 000:Input 001:Output 010:SDC0_D1 011:JTAG_MS 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.22.2.38. PF Configure Register 1 (Default Value: 0x00000000)

Offset: 0xB8			Register Name: **PF_CFG1_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.39. PF Configure Register 2(Default Value: 0x00000000)

Offset: 0xBC			Register Name: **PF_CFG2_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.40. PF Configure Register 3(Default Value: 0x00000000)

Offset: 0xC0			Register Name: **PF_CFG3_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.41. PF Data Register (Default Value: 0x00000000)

Offset: 0xC4			Register Name: **PF_DATA_REG**
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:0	R/W	0x0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If

			the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.22.2.42. PF Multi-Driving Register 0 (Default Value: 0x00001555)

Offset: 0xC8			Register Name: **PF_DRV0_REG**
Bit	R/W	Default/Hex	Description
31:14	/	/	/
[2i+1:2i] (i=0~6)	R/W	0x1	PF_DRV PF[n] Multi-Driving SELECT (n = 0~6) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.2.43. PF Multi-Driving Register 1 (Default Value: 0x00000000)

Offset: 0xCC			Register Name: **PF_DRV1_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.44. PF PULL Register 0 (Default Value: 0x00000000)

Offset: 0xD0			Register Name: **PF_PULL0_REG**
Bit	R/W	Default/Hex	Description
31:14	/	/	/
[2i+1:2i] (i=0~6)	R/W	0x0	PF_PULL PF[n] Pull-up/down Select (n = 0~6) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.2.45. PF PULL Register 1 (Default Value: 0x00000000)

Offset: 0xD4			Register Name: **PF_PULL1_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.46. PG Configure Register 0 (Default Value: 0x77777777)

Offset: 0xD8			Register Name: **PG_CFG0_REG**
Bit	R/W	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PG7_SELECT 000:Input 001:Output 010:UART1_RX 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PG6_SELECT 000:Input 001:Output 010:UART1_TX 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PG5_SELECT 000:Input 001:Output 010:SDC1_D3 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PG4_SELECT 000:Input 001:Output 010:SDC1_D2 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PG3_SELECT 000:Input 001:Output 010:SDC1_D1 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PG2_SELECT 000:Input 001:Output 010:SDC1_D0 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PG1_SELECT 000:Input 001:Output 010:SDC1_CMD 011:Reserved

			100:Reserved 101:Reserved 110:PG_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PG0_SELECT 000:Input 001:Output 010:SDC1_CLK 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT0 111:IO Disable

4.22.2.47. PG Configure Register 1 (Default Value: 0x00777777)

Offset: 0xDC			Register Name: **PG_CFG1_REG**
Bit	R/W	Default/Hex	Description
31:23	/	/	/
22:20	R/W	0x7	PG13_SELECT 000:Input 001:Output 010: PCM1_DIN 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT13 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PG12_SELECT 000:Input 001:Output 010: PCM1_DOUT 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT12 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PG11_SELECT 000:Input 001:Output 010: PCM1_CLK 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT11 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PG10_SELECT 000:Input 001:Output 010: PCM1_CLK 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT10 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PG9_SELECT 000:Input 001:Output 010:UART1_CTS 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT9 111:IO Disable
3	/	/	/

2:0	R/W	0x7	PG8_SELECT 000:Input 001:Output 010:UART1_RTS 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT8 111:IO Disable

4.22.2.48. PG Configure Register 2 (Default Value: 0x00000000)

Offset: 0xE0			Register Name: **PG_CFG2_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.49. PG Configure Register 3 (Default Value: 0x00000000)

Offset: 0xE4			Register Name: **PG_CFG3_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.50. PG Data Register (Default Value: 0x00000000)

Offset: 0xE8			Register Name: **PG_DATA_REG**
Bit	R/W	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.22.2.51. PG Multi-Driving Register 0 (Default Value: 0x05555555)

Offset: 0xEC			Register Name: **PG_DRV0_REG**
Bit	R/W	Default/Hex	Description
31:28	/	/	/
[2i+1:2i] (i=0~13)	R/W	0x1	PF_DRV PF[n] Multi-Driving SELECT (n = 0~13) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.2.52. PG Multi-Driving Register 1 (Default Value: 0x00000000)

Offset: 0xF0			Register Name: **PG_DRV1_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.53. PG PULL Register 0 (Default Value: 0x00000000)

Offset: 0xF4			Register Name: **PG_PULL0_REG**
Bit	R/W	Default/Hex	Description
31:28	/	/	/
[2i+1:2i] (i=0~13)	R/W	0x0	PF_PULL PF[n] Pull-up/down Select (n = 0~13) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.2.54. PG PULL Register 1 (Default Value: 0x00000000)

Offset: 0xF8			Register Name: **PG_PULL1_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.55. PA External Interrupt Configure Register 0 (Default Value: 0x00000000)

Offset: 0x200			Register Name: **PA_EINT_CFG0_REG**
Bit	R/W	Default/Hex	Description
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

4.22.2.56. PA External Interrupt Configure Register 1 (Default Value: 0x00000000)

Offset: 0x204			Register Name: **PA_EINT_CFG1_REG**
Bit	R/W	Default/Hex	Description

[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 8~15) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

4.22.2.57. PA External Interrupt Configure Register 2 (Default Value: 0x00000000)

Offset: 0x208			Register Name: **PA_EINT_CFG2_REG**
Bit	R/W	Default/Hex	Description
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 16~21) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

4.22.2.58. PA External Interrupt Configure Register 3 (Default Value: 0x00000000)

Offset: 0x20C			Register Name: **PA_EINT_CFG3_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.59. PA External Interrupt Control Register (Default Value: 0x00000000)

Offset: 0x210			Register Name: **PA_EINT_CTL_REG**
Bit	R/W	Default/Hex	Description
31:24	/	/	/
[n] (n=0~23)	R/W	0	EINT_CTL External INTn Enable (n = 0~21) 0: Disable 1: Enable

4.22.2.60. PA External Interrupt Status Register (Default Value: 0x00000000)

Offset: 0x214			Register Name: **PA_EINT_STATUS_REG**
Bit	R/W	Default/Hex	Description
31:24	/	/	/
[n] (n=0~23)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~21) 0: No IRQ pending 1: IRQ pending Write '1' to clear

4.22.2.61. PA External Interrupt Debounce Register (Default Value: 0x00000000)

Offset: 0x218			Register Name: **PA_EINT_DEB_REG**
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

4.22.2.62. PG External Interrupt Configure Register 0 (Default Value: 0x00000000)

Offset: 0x220			Register Name: **PG_EINT_CFG0_REG**
Bit	R/W	Default/Hex	Description
31:12	/	/	/
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

4.22.2.63. PG External Interrupt Configure Register 1 (Default Value: 0x00000000)

Offset: 0x224			Register Name: **PG_EINT_CFG1_REG**
Bit	R/W	Default/Hex	Description
31:24	/	/	/
[4i+3:4i] (i=0~5)	R/W	0	EINT_CFG External INTn Mode (n = 8~13) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

4.22.2.64. PG External Interrupt Configure Register 2 (Default Value: 0x00000000)

Offset: 0x228			Register Name: **PG_EINT_CFG2_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.65. PG External Interrupt Configure Register 3 (Default Value: 0x00000000)

Offset: 0x22C			Register Name: **PG_EINT_CFG3_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.22.2.66. PG External Interrupt Control Register (Default Value: 0x00000000)

Offset: 0x230			Register Name: **PG_EINT_CTL_REG**
Bit	R/W	Default/Hex	Description
31:14	/	/	/
[n] (n=0~13)	R/W	0	EINT_CTL External INTn Enable (n = 0~13) 0: Disable 1: Enable

4.22.2.67. PG External Interrupt Status Register (Default Value: 0x00000000)

Offset: 0x234			Register Name: **PG_EINT_STATUS_REG**
Bit	R/W	Default/Hex	Description

31:14	/	/	/
[n] (n=0~13)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~13) 0: No IRQ pending 1: IRQ pending Write '1' to clear

4.22.2.68. PG External Interrupt Debounce Register (Default Value: 0x00000000)

Offset: 0x238			Register Name: **PG_EINT_DEB_REG**
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

4.23. Port Controller(CPUs-PORT)

The chip has 1 port for multi-functional input/out pins. They are shown below:

- Port L(PL):12 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions not used. The external PIO interrupt sources are supported and interrupt mode can be configured by software.

4.23.1. Port Controller Register List

Module Name	Base Address
PIO	0x01F02C00

Register Name	Offset	Description
PL_CFG0	0*0x24+0x00	Port L Configure Register 0
PL_CFG1	0*0x24+0x04	Port L Configure Register 1
PL_CFG2	0*0x24+0x08	Port L Configure Register 2
PL_CFG3	0*0x24+0x0C	Port L Configure Register 3
PL_DAT	0*0x24+0x10	Port L Data Register
PL_DRV0	0*0x24+0x14	Port L Multi-Driving Register 0
PL_DRV1	0*0x24+0x18	Port L Multi-Driving Register 1
PL_PUL0	0*0x24+0x1C	Port L Pull Register 0
PL_PUL1	0*0x24+0x20	Port L Pull Register 1
PL_INT_CFG0	0x200+0*0x20+0x00	PIO Interrrupt Configure Register 0
PL _INT_CFG1	0x200+0*0x20+0x04	PIO Interrrupt Configure Register 1
PL _INT_CFG2	0x200+0*0x20+0x08	PIO Interrrupt Configure Register 2
PL _INT_CFG3	0x200+0*0x20+0x0C	PIO Interrrupt Configure Register 3
PL _INT_CTL	0x200+0*0x20+0x10	PIO Interrupt Control Register
PL _INT_STA	0x200+0*0x20+0x14	PIO Interrupt Status Register
PL _INT_DEB	0x200+0*0x20+0x18	PIO Interrupt Debounce Register

4.23.2. Port Controller Register Description

4.23.2.1. PL Configure Register 0 (Default Value: 0x77777777)

Offset: 0x00			Register Name: **PL_CFG0_REG**
Bit	R/W	Default/Hex	Description
31	/	/	/

			PL7_SELECT	
			000:Input	001:Output
			010:S_JTAG_DI	011:Reserved
			100:Reserved	101:Reserved
30:28	R/W	0x7	110:S_PL_EINT7	111:IO Disable
27	/	/	/	
			PL6_SELECT	
			000:Input	001:Output
			010:S_JTAG_DO	011:Reserved
			100:Reserved	101:Reserved
26:24	R/W	0x7	110:S_PL_EINT6	111:IO Disable
23	/	/	/	
			PL5_SELECT	
			000:Input	001:Output
			010:S_JTAG_CK	011:Reserved
			100:Reserved	101:Reserved
22:20	R/W	0x7	110:S_PL_EINT5	111:IO Disable
19	/	/	/	
			PL4_SELECT	
			000:Input	001:Output
			010:S_JTAG_MS	011:Reserved
			100:Reserved	101:Reserved
18:16	R/W	0x7	110:S_PL_EINT4	111:IO Disable
15	/	/	/	
			PL3_SELECT	
			000:Input	001:Output
			010:S_UART_RX	011:Reserved
			100:Reserved	101:Reserved
14:12	R/W	0x7	110:S_PL_EINT3	111:IO Disable
11	/	/	/	
			PL2_SELECT	
			000:Input	001:Output
			010:S_UART_TX	011:Reserved
			100:Reserved	101:Reserved
10:8	R/W	0x7	110:S_PL_EINT2	111:IO Disable
7	/	/	/	
			PL1_SELECT	
			000:Input	001:Output
			010:S_TWI_SDA	011:Reserved
			100:Reserved	101:Reserved
6:4	R/W	0x7	110:S_PL_EINT1	111:IO Disable
3	/	/	/	
			PL0_SELECT	
			000:Input	001:Output
2:0	R/W	0x7	010:S_TWI_SCK	011:Reserved

			100:Reserved	101:Reserved
			110:S_PL_EINT0	111:IO Disable

4.23.2.2. PL Configure Register 1 (Default Value: 0x00007777)

Offset: 0x04			Register Name: **PL_CFG1_REG**	
Bit	R/W	Default/Hex	Description	
31:15	/	/	/	
14:12	R/W	0x7	PL11_SELECT 000:Input 010:S_CIR_RX 100:Reserved 110:S_PL_EINT11	001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PL10_SELECT 000:Input 010:S_PWM 100:Reserved 110:S_PL_EINT10	001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PL9_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PL_EINT9	001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PL8_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PL_EINT8	001:Output 011:Reserved 101:Reserved 111:IO Disable

4.23.2.3. PL Configure Register 2 (Default Value: 0x00000000)

Offset: 0x08			Register Name: **PL_CFG2_REG**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.23.2.4. PL Configure Register 3 (Default Value: 0x00000000)

Offset: 0x0C			Register Name: **PL_CFG3_REG**
Bit	R/W	Default/Hex	Description

31:0	/	/	/

4.23.2.5. PL Data Register (Default Value: 0x00000000)

Offset: 0x10			Register Name: **PL_DATA_REG**
Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0	PL_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.23.2.6. PL Multi-Driving Register 0 (Default Value: 0x00555555)

Offset: 0x14			Register Name: **PL_DRV0**
Bit	R/W	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PL_DRV PL[n] Multi-Driving Select (n = 0~11) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.23.2.7. PL Multi-Driving Register 1 (Default Value: 0x00000000)

Offset: 0x18			Register Name: **PL_DRV1**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.23.2.8. PL PULL Register 0 (Default Value: 0x00000005)

Offset: 0x1C			Register Name: **PL_PULL0**
Bit	R/W	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x5	PL_PULL PL[n] Pull-up/down Select (n = 0~11) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.23.2.9. PL PULL Register 1 (Default Value: 0x00000000)

Offset: 0x20			Register Name: **PL_PULL1**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.23.2.10. PL External Interrupt Configure Register 0 (Default Value: 0x00000000)

Offset: 0x200			Register Name: **PL_EINT_CFG0**
Bit	R/W	Default/Hex	Description
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

4.23.2.11. PL External Interrupt Configure Register 1 (Default Value: 0x00000000)

Offset: 0x204			Register Name: **PL_EINT_CFG1**
Bit	R/W	Default/Hex	Description
31:20	/	/	/
[4i+3:4i] (i=0~4)	R/W	0	EINT_CFG External INTn Mode (n = 8~11) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

4.23.2.12. PL External Interrupt Configure Register 2 (Default Value: 0x00000000)

Offset: 0x208			Register Name: **PL_EINT_CFG2**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.23.2.13. PL External Interrupt Configure Register 3 (Default Value: 0x00000000)

Offset: 0x20C			Register Name: **PL_EINT_CFG3**
Bit	R/W	Default/Hex	Description
31:0	/	/	/

4.23.2.14. PL External Interrupt Control Register (Default Value: 0x00000000)

Offset: 0x210			Register Name: **PL_EINT_CTL**
Bit	R/W	Default/Hex	Description
31:12	/	/	/
[n] (n=0~11)	R/W	0	EINT_CTL External INTn Enable (n = 0~11) 0: Disable 1: Enable

4.23.2.15. PL External Interrupt Status Register (Default Value: 0x00000000)

Offset: 0x214			Register Name: **PL_EINT_STATUS**
Bit	R/W	Default/Hex	Description
31:12	/	/	/
[n] (n=0~11)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~11) 0: No IRQ pending 1: IRQ pending Write '1' to clear

4.23.2.16. PL External Interrupt Debounce Register (Default Value: 0x00000000)

Offset: 0x218			Register Name: **PL_EINT_DEB**
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

