4.21. Port Controller(CPUx-PORT)

4.21.1. Overview

The chip has 7 ports for multi-functional input/out pins. They are shown below:

- Port A(PA): 22 input/output port
- Port C(PC): 17 input/output port
- Port D(PD): 18 input/output port
- Port E(PE) : 16 input/output port
- Port F(PF) : 7 input/output port
- Port G(PG) : 14 input/output port
- Port L(PL) : 12 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions are not used. The total 3 group external PIO interrupt sources are supported and interrupt mode can be configured by software.

4.21.2. Register List

Module Name	Base Address
PIO	0x01C20800

Register Name	Offset	Description
Pn_CFG0	0x0000 + n*0x24	Port n Configure Register 0 (n from 0 to 6)
Pn_CFG1	0x0004 + n*0x24	Port n Configure Register 1 (n from 0 to 6)
Pn_CFG2	0x0008 + n*0x24	Port n Configure Register 2 (n from 0 to 6)
Pn_CFG3	0x000C + n*0x24	Port n Configure Register 3 (n from 0 to 6)
Pn_DAT	0x0010 + n*0x24	Port n Data Register (n from 0 to 6)
Pn_DRV0	0x0014 + n*0x24	Port n Multi-Driving Register 0 (n from 0 to 6)
Pn_DRV1	0x0018 + n*0x24	Port n Multi-Driving Register 1 (n from 0 to 6)
Pn_PUL0	0x001C + n*0x24	Port n Pull Register 0 (n from 0 to 6)
Pn_PUL1	0x0020 + n*0x24	Port n Pull Register 1 (n from 0 to 6)
PA_INT_CFG0	0x0200 + 0x00 + 0*0x20	PIO Interrrupt Configure Register 0
PA _INT_CFG1	0x0200 + 0x04 + 0*0x20	PIO Interrrupt Configure Register 1
PA _INT_CFG2	0x0200 + 0x08 + 0*0x20	PIO Interrrupt Configure Register 2
PA _INT_CFG3	0x0200 + 0x0C + 0*0x20	PIO Interrrupt Configure Register 3
PA _INT_CTL	0x0200 + 0x10 + 0*0x20	PIO Interrupt Control Register
PA _INT_STA	0x0200 + 0x14 + 0*0x20	PIO Interrupt Status Register
PA_INT_DEB	0x0200 + 0x18 + 0*0x20	PIO Interrupt Debounce Register
PF_INT_CFG0	0x0200 + 0x00 + 1*0x20	PIO Interrrupt Configure Register 0

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PF_INT_CFG1	0x0200 + 0x04 + 1*0x20	PIO Interrrupt Configure Register 1
PF_INT_CFG2	0x0200 + 0x08 + 1*0x20	PIO Interrrupt Configure Register 2
PF_INT_CFG3	0x0200 + 0x0C + 1*0x20	PIO Interrrupt Configure Register 3
PF_INT_CTL	0x0200 + 0x10 + 1*0x20	PIO Interrupt Control Register
PF_INT_STA	0x0200 + 0x14 + 1*0x20	PIO Interrupt Status Register
PF_INT_DEB	0x0200 + 0x18 + 1*0x20	PIO Interrupt Debounce Register
PG_INT_CFG0	0x0200 + 0x00 + 2*0x20	PIO Interrrupt Configure Register 0
PG _INT_CFG1	0x0200 + 0x04 + 2*0x20	PIO Interrrupt Configure Register 1
PG _INT_CFG2	0x0200 + 0x08 + 2*0x20	PIO Interrrupt Configure Register 2
PG _INT_CFG3	0x0200 + 0x0C + 2*0x20	PIO Interrrupt Configure Register 3
PG _INT_CTL	0x0200 + 0x10 + 2*0x20	PIO Interrupt Control Register
PG _INT_STA	0x0200 + 0x14 + 2*0x20	PIO Interrupt Status Register
PG _INT_DEB	0x0200 + 0x18 + 2*0x20	PIO Interrupt Debounce Register

4.21.3. Register Description

4.21.3.1. PA Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0000			**Register Name: PA_CFG0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PA7_SELECT 000:Input 001:Output 010:SIM0_CLK 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PA6_SELECT 000:Input 001:Output 010:SIM0_PWREN 011:PCM0_MCLK 100:Reserved 101:Reserved 110:PA_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PA5_SELECT 000:Input 001:Output 010:UART0_RX 011:PWM0 100:Reserved 101:Reserved 110:PA_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PA4_SELECT

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			000:Input 001:Output 010:UART0_TX 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PA3_SELECT 000:Input 001:Output 010:UART2_CTS 011:JTAG_DI 100:Reserved 101:Reserved 110:PA_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PA2_SELECT 000:Input 001:Output 010:UART2_RTS 011:JTAG_DO 100:Reserved 101:Reserved 110:PA_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PA1_SELECT 000:Input 001:Output 010:UART2_RX 011:JTAG_CK 100:Reserved 101:Reserved 110:PA_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PA0_SELECT 000:Input 001:Output 010:UART2_TX 011:JTAG_MS 100:Reserved 101:Reserved 110:PA_EINT0 111:IO Disable

4.21.3.2. PA Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0004			Register Name: PA_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PA15_SELECT 000:Input 001:Output 010:SPI1_MOSI 011:UART3_RTS 100:Reserved 101:Reserved

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			110:PA_EINT15 111:IO Disable
27	/	/	
26:24	R/W	0x7	PA14_SELECT 000:Input 001:Output 010:SPI1_CLK 011:UART3_RX 100:Reserved 101:Reserved 110:PA_EINT14 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PA13_SELECT 000:Input 001:Output 010:SPI1_CS 011:UART3_TX 100:Reserved 101:Reserved 110:PA_EINT13 111:IO Disable
19	/	/	
18:16	R/W	0x7	PA12_SELECT 000:Input 001:Output 010:TWI0_SDA 011:DI_RX 100:Reserved 101:Reserved 110:PA_EINT12 111:IO Disable
15	/	/	
14:12	R/W	0x7	PA11_SELECT 000:Input 001:Output 010:TWI0_SCK 011:DI_TX 100:Reserved 101:Reserved 110:PA_EINT11 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PA10_SELECT 000:Input 001:Output 010:SIM0_DET 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT10 111:IO Disable
7	/	/	
6:4	R/W	0x7	PA9_SELECT 000:Input 001:Output 010:SIM0_RST 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT9 111:IO Disable
3	/	/	
2:0	R/W	0x7	PA8_SELECT

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			000:Input 001:Output 010:SIM0_DATA 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT8 111:IO Disable

4.21.3.3. PA Configure Register 2 (Default Value: 0x0077_7777)

Offset: 0x0008			Register Name: PA_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	
22:20	R/W	0x7	PA21_SELECT 000:Input 001:Output 010:PCM0_DIN 011:SIM0_VPPPP 100:Reserved 101:Reserved 110:PA_EINT21 111:IO Disable
19	/	/	
18:16	R/W	0x7	PA20_SELECT 000:Input 001:Output 010:PCM0_DOUT 011:SIM0_VPPEN 100:Reserved 101:Reserved 110:PA_EINT20 111:IO Disable
15	/	/	
14:12	R/W	0x7	PA19_SELECT 000:Input 001:Output 010:PCM0_CLK 011:TWI1_SDA 100:Reserved 101:Reserved 110:PA_EINT19 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PA18_SELECT 000:Input 001:Output 010:PCM0_SYNC 011:TWI1_SCK 100:Reserved 101:Reserved 110:PA_EINT18 111:IO Disable
7	/	/	
6:4	R/W	0x7	PA17_SELECT 000:Input 001:Output 010:OWA_OUT 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT17 111:IO Disable

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3	/	/	
2:0	R/W	0x7	PA16_SELECT 000:Input 001:Output 010:SPI1_MISO 011:UART3_CTS 100:Reserved 101:Reserved 110:PA_EINT16 111:IO Disable

4.21.3.4. PA Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PA_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.5. PA Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PA_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:0	R/W	0x0	PA_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.21.3.6. PA Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0014			Register Name: PA_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.7. PA Multi-Driving Register 1 (Default Value: 0x0000_0555)

Offset: 0x0018			Register Name: PA_DRV1 _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[2i+1:2i]	R/W	0x1	PA_DRV

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(i=0~5)			PA[n] Multi-Driving Select (n = 16~21) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.8. PA PULL Register 0 (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: PA_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.9. PA PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PA_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 16~21) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.10. PC Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0048			Register Name: PC_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PC7_SELECT 000:Input 001:Output 010:NAND_RB1 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PC6_SELECT

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			000:Input 001:Output 010:NAND_RB0 011:SDC2_CMD 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PC5_SELECT 000:Input 001:Output 010:NAND_RE 011:SDC2_CLK 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PC4_SELECT 000:Input 001:Output 010:NAND_CE0 011:Reserved 100:SPI0_MISO 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PC3_SELECT 000:Input 001:Output 010:NAND_CE1 011:SPI0_CS 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PC2_SELECT 000:Input 001:Output 010:NAND_CLE 011:SPI0_CLK 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PC1_SELECT 000:Input 001:Output 010:NAND_ALE 011:SPI0_MISO 100:SDC2_DS 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/

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2:0	R/W	0x7	PC0_SELECT 000:Input 001:Output 010:NAND_WE 011:SPI0_MOSI 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.21.3.11. PC Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x004C			Register Name: PC_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PC15_SELECT 000:Input 001:Output 010:NAND_DQ7 011:SDC2_D7 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PC14_SELECT 000:Input 001:Output 010:NAND_DQ6 011:SDC2_D6 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PC13_SELECT 000:Input 001:Output 010:NAND_DQ5 011:SDC2_D5 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PC12_SELECT 000:Input 001:Output 010:NAND_DQ4 011:SDC2_D4 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PC11_SELECT 000:Input 001:Output 010:NAND_DQ3 011:SDC2_D3 100:Reserved 101:Reserved

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			110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PC10_SELECT 000:Input 001:Output 010:NAND_DQ2 011:SDC2_D2 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PC9_SELECT 000:Input 001:Output 010:NAND_DQ1 011:SDC2_D1 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PC8_SELECT 000:Input 001:Output 010:NAND_DQ0 011:SDC2_D0 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.21.3.12. PC Configure Register 2 (Default Value: 0x0000_0777)

Offset: 0x0050			Register Name: PC_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:8	R/W	0x7	/
7	/	/	/
6:4	R/W	0x7	/
3	/	/	/
2:0	R/W	0x7	PC16_SELECT 000:Input 001:Output 010:NAND_DQS 011:SDC2_RST 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.21.3.13. PC Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: PC_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	/	/	/

4.21.3.14. PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PC_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.21.3.15. PC Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x005C			Register Name: PC_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PC_DRV PC[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.16. PC Multi-Driving Register 1 (Default Value: 0x0000_0015)

Offset: 0x0060			Register Name: PC_DRV1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
[2i+1:2i] (i=0~2)	R/W	0x1	PC_DRV PC[n] Multi-Driving Select (n = 16~18) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.17. PC PULL Register 0 (Default Value: 0x0000_5140)

Offset: 0x0064			Register Name: PC_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x5140	PC_PULL PC[n] Pull-up/down Select (n = 0~15)

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			00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.18. PC PULL Register 1 (Default Value: 0x0000_0014)

Offset: 0x0068			Register Name: PC_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	Reserved
[2i+1:2i] (i=0~2)	R/W	0x14	PC_PULL PC[n] Pull-up/down Select (n = 16~18) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.19. PD Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x006C			Register Name: PD_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PD7_SELECT 000:Input 001:Output 010:RGMII_TXD3/MII_TXD3/RMII_NULL 011:Reserved 100:TS2_D3 101:TS3_CLK 110:Reserved 111:IO Disable
27	/	/	Reserved
26:24	R/W	0x7	PD6_SELECT 000:Input 001:Output 010:RGMII_NULL/MII_RXERR/RMII_RXER 011:Reserved 100:TS2_D2 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PD5_SELECT 000:Input 001:Output 010:RGMII_RXCTL/MII_RXDV/RMII_CRS_DV 011:Reserved 100:TS2_D1 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PD4_SELECT 000:Input 001:Output

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			010:RGMII_RXCK/MII_RXCK/RMII_NULL 011:Reserved 100:TS2_D0 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PD3_SELECT 000:Input 001:Output 010:RGMII_RXD0/MII_RXD0/RMII_RXD0 011:Reserved 100:TS2_DVLD 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PD2_SELECT 000:Input 001:Output 010:RGMII_RXD1/MII_RXD1/RMII_RXD1 011:Reserved 100:TS2_SYNC 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PD1_SELECT 000:Input 001:Output 010:RGMII_RXD2/MII_RXD2/RMII_NULL 011:DI_RX 100:TS2_ERR 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD0_SELECT 000:Input 001:Output 010:RGMII_RXD3/MII_RXD3/RMII_NULL 011:DI_TX 100:TS2_CLK 101:Reserved 110:Reserved 111:IO Disable

4.21.3.20. PD Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0070			Register Name: PD_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PD15_SELECT 000:Input 001:Output 010:RGMII_CLKIN/MII_COL/RMII_NULL 011:Reserved 100:SIM1_RST 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/

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26:24	R/W	0x7	PD14_SELECT 000:Input 001:Output 010:RGMII_NULL/MII_TXERR/RMII_NULL 011:Reserved 100:SIM1_DATA 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PD13_SELECT 000:Input 001:Output 010:RGMII_TXCTL/MII_TXEN/RMII_TXEN 011:Reserved 100:SIM1_CLK 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PD12_SELECT 000:Input 001:Output 010:RGMII_TXCK/MII_TXCK/RMII_TXCK 011:Reserved 100:SIM1_PWREN 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PD11_SELECT 000:Input 001:Output 010:RGMII_NULL/MII_CRS/RMII_NULL 011:Reserved 100:TS2_D7 101:TS3_D0 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PD10_SELECT 000:Input 001:Output 010:RGMII_TXD0/MII_TXD0/RMII_TXD0 011:Reserved 100:TS2_D6 101:TS3_DVLD 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PD9_SELECT 000:Input 001:Output 010:RGMII_TXD1/MII_TXD1/RMII_TXD1 011:Reserved 100:TS2_D5 101:TS3_SYNC 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD8_SELECT 000:Input 001:Output 010:RGMII_TXD2/MII_TXD2/RMII_NULL 011:Reserved

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			100:TS2_D4 110:Reserved	101:TS3_ERR 111:IO Disable

4.21.3.21. PD Configure Register 2 (Default Value: 0x0000_0077)

Offset: 0x0074			Register Name: PD_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x7	PD17_SELECT 000:Input 001:Output 010:MDIO 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD16_SELECT 000:Input 001:Output 010:MDC 011:Reserved 100:SIM1_DET 101:Reserved 110:Reserved 111:IO Disable

4.21.3.22. PD Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: PD_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.23. PD Data Register (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: PD_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R/W	0x0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

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4.21.3.24. PD Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0080			Register Name: PD_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PD_DRV PD[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.25. PD Multi-Driving Register 1 (Default Value: 0x0000_0005)

Offset: 0x0084			Register Name: PD_DRV1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
[2i+1:2i] (i=0~1)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 16~17) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.26. PD PULL Register 0 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: PD_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.27. PD PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: PD_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	Reserved
[2i+1:2i] (i=0~1)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 16~17) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

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4.21.3.28. PE Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0090			Register Name: PE_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PE7_SELECT 000:Input 001:Output 010:CSI_D3 011:TS0_D3 100:TS1_CLK 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PE6_SELECT 000:Input 001:Output 010:CSI_D2 011:TS0_D2 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PE5_SELECT 000:Input 001:Output 010:CSI_D1 011:TS0_D1 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PE4_SELECT 000:Input 001:Output 010:CSI_D0 011:TS0_D0 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PE3_SELECT 000:Input 001:Output 010:CSI_VSYNC 011:TS0_DVLD 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PE2_SELECT 000:Input 001:Output 010:CSI_HSYNC 011:TS0_SYNC 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

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7	/	/	/
6:4	R/W	0x7	PE1_SELECT 000:Input 001:Output 010:CSI_MCLK 011:TS0_ERR 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PE0_SELECT 000:Input 001:Output 010:CSI_PCLK 011:TS0_CLK 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.21.3.29. PE Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0094			Register Name: PE_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PE15_SELECT 000:Input 001:Output 010:Reserved 011:SIM1_VPPPP 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PE14_SELECT 000:Input 001:Output 010:Reserved 011:SIM1_VPPEN 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PE13_SELECT 000:Input 001:Output 010:CSI_SDA 011:TWI2_SDA 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PE12_SELECT 000:Input 001:Output 010:CSI_SCK 011:TWI2_SCK

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			100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PE11_SELECT 000:Input 001:Output 010:CSI_D7 011:TS0_D7 100:TS1_D0 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PE10_SELECT 000:Input 001:Output 010:CSI_D6 011:TS0_D6 100:TS1_DVLD 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PE9_SELECT 000:Input 001:Output 010:CSI_D5 011:TS0_D5 100:TS1_SYNC 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PE8_SELECT 000:Input 001:Output 010:CSI_D4 011:TS0_D4 100:TS1_ERR 101:Reserved 110:Reserved 111:IO Disable

4.21.3.30. PE Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0098			**Register Name: PE_CFG2_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.31. PE Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x009C			**Register Name: PE_CFG3_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

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4.21.3.32. PE Data Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: PE_DATA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.21.3.33. PE Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x00A4			Register Name: PE_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PE_DRV PE[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.34. PE Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: PE_DRV1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.35. PE PULL Register 0 (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: PE_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PE_PULL PE[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.36. PE PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: PE_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	/	/	/

4.21.3.37. PF Configure Register 0 (Default Value: 0x0777_7777)

Offset: 0x00B4			Register Name: PF_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x7	PF6_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:Reserved 110:PF_EINT6 111:IO Disable
23			
22:20	R/W	0x7	PF5_SELECT 000:Input 001:Output 010:SDC0_D2 011:JTAG_CK 100:Reserved 101:Reserved 110:PF_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PF4_SELECT 000:Input 001:Output 010:SDC0_D3 011:UART0_RX 100:Reserved 101:Reserved 110:PF_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PF3_SELECT 000:Input 001:Output 010:SDC0_CMD 011:JTAG_DO 100:Reserved 101:Reserved 110:PF_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PF2_SELECT 000:Input 001:Output 010:SDC0_CLK 011:UART0_TX 100:Reserved 101:Reserved 110:PF_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PF1_SELECT 000:Input 001:Output

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			010:SDC0_D0 011:JTAG_DI 100:Reserved 101:Reserved 110:PF_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PF0_SELECT 000:Input 001:Output 010:SDC0_D1 011:JTAG_MS 100:Reserved 101:Reserved 110:PF_EINT0 111:IO Disable

4.21.3.38. PF Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: PF_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.39. PF Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: PF_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.40. PF Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: PF_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.41. PF Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: PF_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R/W	0x0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

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4.21.3.42. PF Multi-Driving Register 0 (Default Value: 0x0000_1555)

Offset: 0x00C8			Register Name: PF_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
[2i+1:2i] (i=0~6)	R/W	0x1	PF_DRV PF[n] Multi-Driving SELECT (n = 0~6) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.43. PF Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: PF_DRV1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.44. PF PULL Register 0 (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PF_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
[2i+1:2i] (i=0~6)	R/W	0x0	PF_PULL PF[n] Pull-up/down Select (n = 0~6) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.45. PF PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name: PF_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.46. PG Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00D8			Register Name: PG_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PG7_SELECT

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			000:Input 001:Output 010:UART1_RX 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PG6_SELECT 000:Input 001:Output 010:UART1_TX 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PG5_SELECT 000:Input 001:Output 010:SDC1_D3 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PG4_SELECT 000:Input 001:Output 010:SDC1_D2 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PG3_SELECT 000:Input 001:Output 010:SDC1_D1 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PG2_SELECT 000:Input 001:Output 010:SDC1_D0 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PG1_SELECT 000:Input 001:Output 010:SDC1_CMD 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT1 111:IO Disable

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3	/	/	/
2:0	R/W	0x7	PG0_SELECT 000:Input 001:Output 010:SDC1_CLK 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT0 111:IO Disable

4.21.3.47. PG Configure Register 1 (Default Value: 0x0077_7777)

Offset: 0x00DC			Register Name: PG_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x7	PG13_SELECT 000:Input 001:Output 010: PCM1_DIN 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT13 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PG12_SELECT 000:Input 001:Output 010: PCM1_DOUT 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT12 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PG11_SELECT 000:Input 001:Output 010: PCM1_CLK 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT11 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PG10_SELECT 000:Input 001:Output 010: PCM1_SYNC 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT10 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PG9_SELECT 000:Input 001:Output 010:UART1_CTS 011: Reserved

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			100:Reserved 101:Reserved 110:PG_EINT9 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PG8_SELECT 000:Input 001:Output 010:UART1_RTS 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT8 111:IO Disable

4.21.3.48. PG Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: PG_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.49. PG Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: PG_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.50. PG Data Register (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PG_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.21.3.51. PG Multi-Driving Register 0 (Default Value: 0x0555_5555)

Offset: 0x00EC			Register Name: PG_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
[2i+1:2i] (i=0~13)	R/W	0x1	PG_DRV PG[n] Multi-Driving SELECT (n = 0~13)

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			00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.52. PG Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: PG_DRV1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.53. PG PULL Register 0 (Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: PG_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
[2i+1:2i] (i=0~13)	R/W	0x0	PG_PULL PG[n] Pull-up/down Select (n = 0~13) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.54. PG PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: PG_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.55. PA External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PA_EINT_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	EINT_CFG External INTn Mode (n = 0~7) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

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4.21.3.56. PA External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PA_EINT_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	EINT_CFG External INTn Mode (n = 8~15) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.57. PA External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: PA_EINT_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
[4i+3:4i] (i=0~5)	R/W	0x0	EINT_CFG External INTn Mode (n = 16~21) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.58. PA External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: PA_EINT_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.59. PA External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x210			Register Name: PA_EINT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
[n] (n=0~21)	R/W	0x0	EINT_CTL External INTn Enable (n = 0~21)

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			0: Disable 1: Enable

4.21.3.60. PA External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PA_EINT_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
[n] (n=0~21)	R/W1C	0x0	EINT_STATUS External INTn Pending Bit (n = 0~21) 0: No IRQ pending 1: IRQ pending Write '1' to clear it.

4.21.3.61. PA External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PA_EINT_DEB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

4.21.3.62. PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: PF_EINT_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
[4i+3:4i] (i=0~6)	R/W	0x0	EINT_CFG External INTn Mode (n = 0~6) 0000: Positive Edge 0001: Negative Edge

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			0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.63. PF External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: PF_EINT_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.64. PF External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: PF_EINT_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.65. PF External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: PF_EINT_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.66. PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PF_EINT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
[n] (n=0~6)	R/W	0x0	EINT_CTL External INTn Enable (n = 0~6) 0: Disable 1: Enable

4.21.3.67. PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PF_EINT_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
[n] (n=0~6)	R/W1C	0x0	EINT_STATUS External INTn Pending Bit (n = 0~6)

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			0: No IRQ pending 1: IRQ pending Write '1' to clear it

4.21.3.68. PF External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: PF_EINT_DEB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

4.21.3.69. PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: PG_EINT_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	EINT_CFG External INTn Mode (n = 0~7) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.70. PG External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: PG_EINT_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
[4i+3:4i] (i=0~5)	R/W	0x0	EINT_CFG External INTn Mode (n = 8~13)

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			0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.71. PG External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: PG_EINT_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.72. PG External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: PG_EINT_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.73. PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: PG_EINT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
[n] (n=0~13)	R/W	0x0	EINT_CTL External INTn Enable (n = 0~13) 0: Disable 1: Enable

4.21.3.74. PG External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: PG_EINT_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
[n] (n=0~13)	R/W1C	0x0	EINT_STATUS External INTn Pending Bit (n = 0~13) 0: No IRQ pending 1: IRQ pending

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			Write ‘1’ to clear it

4.21.3.75. PG External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: PG_EINT_DEB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

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4.22. Port Controller (CPUs-PORT)

4.22.1. Overview

The chip has 1 port for multi-functional input/out pins. They are shown below:

- Port L(PL):12 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions not used. The external PIO interrupt sources are supported and interrupt mode can be configured by software.

4.22.2. Register List

Module Name	Base Address
PIO	0x01F02C00

Register Name	Offset	Description
PL_CFG0	0x0000	Port L Configure Register 0
PL_CFG1	0x0004	Port L Configure Register 1
PL_CFG2	0x0008	Port L Configure Register 2
PL_CFG3	0x000C	Port L Configure Register 3
PL_DAT	0x0010	Port L Data Register
PL_DRV0	0x0014	Port L Multi-Driving Register 0
PL_DRV1	0x0018	Port L Multi-Driving Register 1
PL_PUL0	0x001C	Port L Pull Register 0
PL_PUL1	0x0020	Port L Pull Register 1
PL_INT_CFG0	0x0200 + 0x00	PIO Interrrupt Configure Register 0
PL_INT_CFG1	0x0200 + 0x04	PIO Interrrupt Configure Register 1
PL_INT_CFG2	0x0200 + 0x08	PIO Interrrupt Configure Register 2
PL_INT_CFG3	0x0200 + 0x0C	PIO Interrrupt Configure Register 3
PL_INT_CTL	0x0200 + 0x10	PIO Interrupt Control Register
PL_INT_STA	0x0200 + 0x14	PIO Interrupt Status Register
PL_INT_DEB	0x0200 + 0x18	PIO Interrupt Debounce Register

4.22.3. Register Description

4.22.3.1. PL Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0000	Register Name: PL_CFG0_REG

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Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PL7_SELECT 000:Input 001:Output 010:S_JTAG_DI 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PL6_SELECT 000:Input 001:Output 010:S_JTAG_DO 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PL5_SELECT 000:Input 001:Output 010:S_JTAG_CK 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PL4_SELECT 000:Input 001:Output 010:S_JTAG_MS 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PL3_SELECT 000:Input 001:Output 010:S_UART_RX 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PL2_SELECT 000:Input 001:Output 010:S_UART_TX 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PL1_SELECT

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			000:Input 001:Output 010:S_TWI_SDA 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PL0_SELECT 000:Input 001:Output 010:S_TWI_SCK 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT0 111:IO Disable

4.22.3.2. PL Configure Register 1 (Default Value: 0x0000_7777)

Offset: 0x0004			Register Name: PL_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x7	PL11_SELECT 000:Input 001:Output 010:S_CIR_RX 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT11 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PL10_SELECT 000:Input 001:Output 010:S_PWM 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT10 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PL9_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT9 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PL8_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT8 111:IO Disable

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4.22.3.3. PL Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: PL_CFG2_REG
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

4.22.3.4. PL Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PL_CFG3_REG
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

4.22.3.5. PL Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PL_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	PL_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.22.3.6. PL Multi-Driving Register 0 (Default Value: 0x0055_5555)

Offset: 0x0014			Register Name: PL_DRV0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PL_DRV PL[n] Multi-Driving Select (n = 0~11) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.3.7. PL Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: PL_DRV1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

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4.22.3.8. PL PULL Register 0 (Default Value: 0x0000_0005)

Offset: 0x001C			Register Name: PL_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x5	PL_PULL PL[n] Pull-up/down Select (n = 0~11) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.3.9. PL PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PL_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.22.3.10. PL External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PL_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	EINT_CFG External INTn Mode (n = 0~7) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.22.3.11. PL External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PL_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
[4i+3:4i] (i=0~3)	R/W	0x0	EINT_CFG External INTn Mode (n = 8~11) 0000: Positive Edge 0001: Negative Edge 0010: High Level

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			0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.22.3.12. PL External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: PL_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.22.3.13. PL External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: PL_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.22.3.14. PL External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PL_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[n] (n=0~11)	R/W	0x0	EINT_CTL External INTn Enable (n = 0~11) 0: Disable 1: Enable

4.22.3.15. PL External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PL_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[n] (n=0~11)	R/W	0x0	EINT_STATUS External INTn Pending Bit (n = 0~11) 0: No IRQ pending 1: IRQ pending Write '1' to clear

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4.22.3.16. PL External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PL_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

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